REMARKS

In response to the above-identified Final Office Action, the Applicant presents the below remarks and respectfully request reconsideration of the application in light of these remarks.

The Examiner rejected claims 1-4, 8-11, and 14-17, and 21-23 under 35 U.S.C. 102(b) as being anticipated by Austin, U.S. Patent No. 3,163,850 (hereinafter Austin). The Examiner also rejected claims 5, 7, 12, 13, 18 and 20 under 35 U.S.C. 103(a) as being unpatentable over Austin. Additionally, the Examiner rejected claims 6 and 19 under 35 U.S.C. 103 (a) as being unpatentable over Austin in view of U.S. Patent 2,968,027 (hereinafter McDonnell). The Applicant respectfully traverses this rejection for the reasons set out below.

Applicant contends that the references individually or in combination do not teach or suggest all limitations of claim 1, or the other independent claims of the present application. The Applicant's arguments shall be presented with respect to claim 1. However, these comments are applicable to the other independent claims of the present application, and the Examiner is respectfully requested to consider these comments and remarks when reviewing the other independent claims for allowability.

Austin does not teach or suggest the present invention, as claimed. Claim 1 reads as follows:

> A method for performing a gather operation on a computer processor comprising:
> computing addresses for a plurality of data elements of a matrix stored in memory utilizing a plurality of indices and a base address;
> retrieving each of said data elements from memory based on the computed addresses; and
> executing a plurality of instructions, each instruction depositing one or more of said data elements contiguously with other data elements in a storage location. (Emphasis added)

Austin does not disclose computing addresses for a plurality of data elements of a matrix stored in memory utilizing a plurality of indices and a base address. In Austin, the first RDW (record definition word) address passes to the Core Address triggers to read out the first RW to the Record Definition register. The address control register is then one-upped by a plus-one adder to address the second RDW. The computation of the next RDW does not include any computation of utilizing a plurality of indices and a base address. Moreover, at no point in Austin is there a disclosure of computing addresses for a plurality of data elements of a matrix stored in memory utilizing a plurality of indices and a base address.

The McDonnell reference is not utilized to invalidate the elements of the independent claims of the present invention, because McDonnell does not teach or suggest the present invention as claimed in, at least, the independent claims.

The Applicant submits that the rejection under 35 U.S.C. § 102 (b) and 103 (a) has been addressed, and withdrawal of this rejection is respectfully requested. The Applicant furthermore submits that all pending claims are in condition for allowance, which is earnestly solicited.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due. Furthermore, if an extension is required, then Applicants hereby request such an extension.

Respectfully submitted,

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Dated: June 20, 2003

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